24<sup>th</sup> International Conference On VLSI Design



10<sup>th</sup> International Conference On Embedded Systems

January 2-7, 2011 Indian Institute of Technology Madras, Chennai, India

# **DESIGN CONTEST**

The aim of the contest is to promote excellence in the design of electronics systems in educational, research and industry establishments by providing a venue for professionals in the field of "VLSI and Embedded System" to showcase their designs. The design contest is open to all. But, we particularly encourage students pursuing project in the colleges and universities to participate.

## Criteria for entry to the design contest in VLSI Conference 2011

For VLSI 2011, we solicit entries for the design contest from full-time graduate and undergraduate students, and professionals from industry and research establishments. The design and implementation should have taken place within 24 months prior to the submission deadline as part of the course, research or development work. It is expected that participants will take necessary clearance from their institutes or organizations. They will need to give a declaration in this regard in specified format.

## Scope

Designs can be for analog, digital, or programmable circuits and systems. Submitted designs can be embodied as digital or analog integrated circuits, programmable processors, SoCs, platform-based or embedded systems designs. Design/project fields include (but not limited to):

- Digital Integrated Circuits
- Analog Integrated Circuits
- FPGA based designs
- Computer Architectures/ Processors
- Reconfigurable Computing Systems
- SoC / Platform-based designs
- Embedded Systems
- MEMS/Optics/Bio-Chips
- Innovative Design Methodolgies and Verification Techniques.

## **Design Categories**

Entries can be in the categories of integrated circuits and electronic systems (boardlevel designs). There will be two categories for evaluating the entries: Operational and Conceptual Designs.

• Operational designs will have been built and tested. For these entries, proof of implementation must be provided in the form of die and board photographs along with measurement data.

 Conceptual designs need not have been implemented but must be thoroughly simulated and should include a detailed test plan.

#### Prize

Award-winning entries will be given attractive cash prizes. Also, each awarded design will be given an opportunity to make a short presentation or demo at a special session of VLSI 2011 conference to be held in January 2011 in Chennai. However, please note that no travel subsidy is available for this purpose.

#### **Evaluation Criteria**

A panel of experts from industry and academia will judge the submissions. Submitted designs will be reviewed in a process similar to the review process for the technical papers. If deemed appropriate, the panel may award entries from students and industry professionals separately. The following list provides some of the criteria that will be applied in the selection of designs:

- Innovative concept / implementation
- Industry / practical application
- Description of the design process
- Reliability of design and implementation
- Performance of the design
- Novelty of application, algorithm, architecture
- Testing strategy (or Simulation for the conceptual category) and results

## **Submission Guidelines**

You may want to address some of the following questions and issues in your Project Report:

System Overview:

- Motivation for designing the chip or system.
- Is the implementation medium appropriate?
- Does this design satisfy the system requirements?
- What is unique about this project?
- What novel ideas or elegant solutions does the design include?
- Implementation and Engineering Considerations:
- Specifications: functional, timing, electrical, and environmental (temperature).
- Trade-offs: architectural and circuit trade-offs, I/O considerations, floorplanning and interconnect approaches. Emphasis should be placed on "why" part.
- Timing and Critical Paths. What clocking scheme is used? Why?
- Which paths are critical? Have you simulated or measured their delays?
- Block Diagram, Logic / Circuit Diagrams, and Algorithms.
- Photo or Final Layout Plot (annotate so various blocks can be identified).
- Verification/Simulation (keep it brief): how did you assure that the chip would work as specified?

Testing:

- How did you, or will you, test this part with I/O pins only?
- What test equipment did you use?
- Actual test results, if available, should be summarized.

#### Statistics:

• Die size, total power, number of transistors, density of layout, maximum clock speed, and/or other relevant parameters.

#### **Submission Format**

VLSI Conference does not require transfer of any 'intellectual property right'. However, it assumes that any submitted design can be publicly shared and any right protection required is done by the participants or their organizations prior to the submission. Please take all permissions / legal sign offs accordingly.

Your submission should meet the following requirements:

1. The cover page must include:

- Title of the design
- Names and email IDs of authors
- Mailing address and mobile number of the contact author
- Area of the application and implementation method
- Contribution of each group, if the prototype is jointly developed with non-academic parties

2. The summary must be written within 4 single spaced pages, including figures, tables, and references. Only Adobe PDF files will be accepted.

3. It is strongly recommended that measured experimental results and a chip micrograph or a photograph of the hardware prototype be included. If the experimental results and the photograph have not been prepared before the deadline of submission, the authors can send the revised paper including them later.

4. Last date of Submission: August 23, 2010

5. Questions to be directed to the Design Contest Chair: <u>Madhavi Rao</u>, Cadence Design Systems (<u>rmadhavi@cadence.com</u>)